Module 4: Concurrency and associated topics in VHDL

Learning objectives:

Study of the following topics -

VHDL architecture description styles: structural, data flow and behavioral

Parallelism and concurrency

This module teaches extremely important concepts in VHDL that set it apart from software programming languages. Different ways of describing a given digital functionality is described in this module. The mechanism of operation of VHDL compilers that enable them to mimic real digital circuits is also discussed here.

First go through the Powerpoint slides and the videos and then complete the associated reading assignments for this module.

Reading assignments

The required reading for understanding module 4 topics is listed below. Use the book: VHDL for Programmable Logic by Kevin Skahill for this purpose.

Start reading from the beginning of chapter 3 and read until you reach section 3.4 on identifiers and data objects, then stop.

Questions

Q1. Do question 3.5 (chapter 3). This question can be seen in the attachment with the submission link for HW4. Please note that if your Boolean equation or gate-level design itself is not 100% correct then that will not make you lose marks. The purpose here is to familiarize you with the different ways you can represent a digital design in VHDL. When actually designing a circuit/system you will select the best way yourself. In this type of problem, that will be through if-then-else or when-else statement, but this problem asks for more just to show you other possibilities in VHDL.

Q2. In no more than 1000 words, explain how VHDL implements parallelism (concurrency) through its simulation cycles.